AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application.

Please cancel claims 3, 4, 11, and 12 without prejudice.

Listing of Claims:

1. (currently amended) A circuit arrangement for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video channel selectably carries either color or monochrome video data, comprising:

a processor configured and arranged to interpret display commands;

a selector circuit coupled to the processor and having a plurality of output ports and input ports arranged for connection to the plurality of video data channels, the selector circuit configured and arranged to select digital video data received at a first data rate from a subset of the channels responsive to an input selection signal from the processor and provide selected digital video data at the output ports at a second data rate that is half the first data rate;

a plurality of data routers, each having an output port and an input port coupled to a respective one of the output ports of the selector circuit, and each data router configured and arranged to convert input video data from YCrCb format to RGB format, wherein the video data is logically segmented into frames of pixel data, and the data routers are configurable for operation in a first mode or a second mode, wherein a single data router processes video data from a single channel of video data while operating in the first mode, and in the second mode a first data router processes a first half of the pixel data of a frame and a second data router processes a second half of the pixel data of the frame;

a video data sequencer coupled to the output ports of the data routers, the sequencer configured and arranged to merge the selected video data into frames of video data; and

a digital-to-analog converter coupled to the video data sequencer, the converter configured and arranged to generate an analog video signal from the frames of video data.

2. (currently amended) The circuit arrangement ~~apparatus~~ of claim 1, wherein each data router is configurable to compress the input video data at selectable compression level.

3. (canceled)

4. (canceled)

5. (original) The circuit arrangement of claim 1, wherein the circuit arrangement is supported on a circuit board having connectors arranged for connecting to the video channels.

6. (original) The circuit arrangement of claim 1, further comprising:

a first memory coupled to the processor and arranged for storage of graphics data to be overlaid on the video data;

a second memory coupled to the sequencer and arranged for storage of the video data; and

a pixel selector having input ports coupled to the first memory and to the second memory and an output port coupled to the digital-to-analog converter, wherein the pixel selector is configured and arranged to select graphics data from the first memory when graphics data is present.

7. (original) The circuit arrangement of claim 6, further comprising:

a third memory coupled to the processor and arranged for storage of a first-level priority graphics data;

a pixel output controller coupled to the third memory and to the video memory, the pixel output controller configured and arranged to sequence output of data from the first and second memories to the pixel selector and sequence first-level priority graphics data from the third memory to the digital-to-analog converter,

wherein the first-level priority graphics data which takes precedence for display over the graphics data of the first memory and over the video data.

8. (original) The circuit arrangement of claim 6, wherein the pixel output controller is further configured and arranged to sequence output of video data from the second memory responsive to window position parameters associated with data from the video sources.

9. (original) The circuit arrangement of claim 6, further comprising a blink-translation circuit coupled to the first memory and to the pixel selector, wherein the blink-translation circuit is configured and arranged to selectively replace an input pixel value with a configurable pixel value at a configurable interval.

10. (currently amended) The circuit arrangement ~~apparatus~~ of claim 6, wherein each data router is configurable to compress the input video data at selectable compression level.

11. (canceled)

12. (canceled)

13. (currently amended) A method for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video channel selectably carries either color or monochrome video data, comprising:

interpreting display commands that select a subset of the video data;

receiving digital video data on the plurality video data channels at a first data rate;

selecting digital video data from a subset of the channels responsive to the display commands and providing as output selected digital video data at the output ports at a second data rate that is half the first data rate;

decoding color and monochrome format video data responsive to configuration signals indicating data formats for the channels;

converting the video data from YCrCb format to RGB format, wherein the video data is logically segmented into frames of pixel data, and the converting includes converting the video data from YCrCb format to RGB format using a single converter for each frame in response to a first operating mode, and converting the frame of video data from YCrCb format to RGB format using a first converter for a first half of the pixel data of the frame and a second converter for a second half of the pixel data of the frame in response to a second operating mode;

merging the selected video data into frames of video data; and

converting the video data to an analog video signal from the frames of video data.

14. (Previously presented) The method of claim 13, further comprising compressing the video data at a selectable compression level responsive to the display commands.

15. (Previously presented) The method of claim 14, further comprising:

storing the video data in a first memory;

storing overlay data in a second memory, wherein the overlay data; and

selecting between the overlay data and the video data for conversion to a video signal.

16. (Previously presented) The method of claim 13, further comprising:

storing the video data in a first memory;

storing overlay data in a second memory, wherein the overlay data; and

selecting between the overlay data and the video data for conversion to a video signal.

17. (Previously presented) The method of claim 13, further comprising:

establishing respective priority levels for the digital video data generated from video signals from the video sources; and

if a portion of the selected video data from a first one of the subset of channels and a portion of the selected video data from a second one of the subset of channels require common storage space in the first memory, then selecting between the portion of the video data from the first channel and the portion of the video data from the second channel responsive to the priority levels.

18. (currently amended) An apparatus for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video channel selectably carries either color or monochrome video data, comprising:

means for interpreting display commands that select a subset of the video data;

means for selecting digital video data from a subset of the channels responsive to the display commands, whereby selected digital video data is provided at the output ports;

means for decoding color and monochrome format video data responsive to configuration signals indicating data formats for the channels;

first and second means for converting the video data from YCrCb format to RGB format, wherein the video data is logically segmented into frames of pixel data, and the first means for converting the video data from YCrCb format to RGB format converts all pixel data of a frame responsive to a first operating mode, and responsive to a second operating mode the first converter converts a first half of the pixel data of the frame and the second converter converts the pixel data of a second half of the frame;

means for merging the selected video data into frames of video data; and

means for converting the video data to an analog video signal from the frames of video data.